**Lab 11**

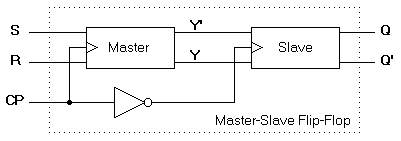
**Lab Task 1:**

**Implement the SR Master-Slave flip flop on logic works. Also, show the timing diagram.**

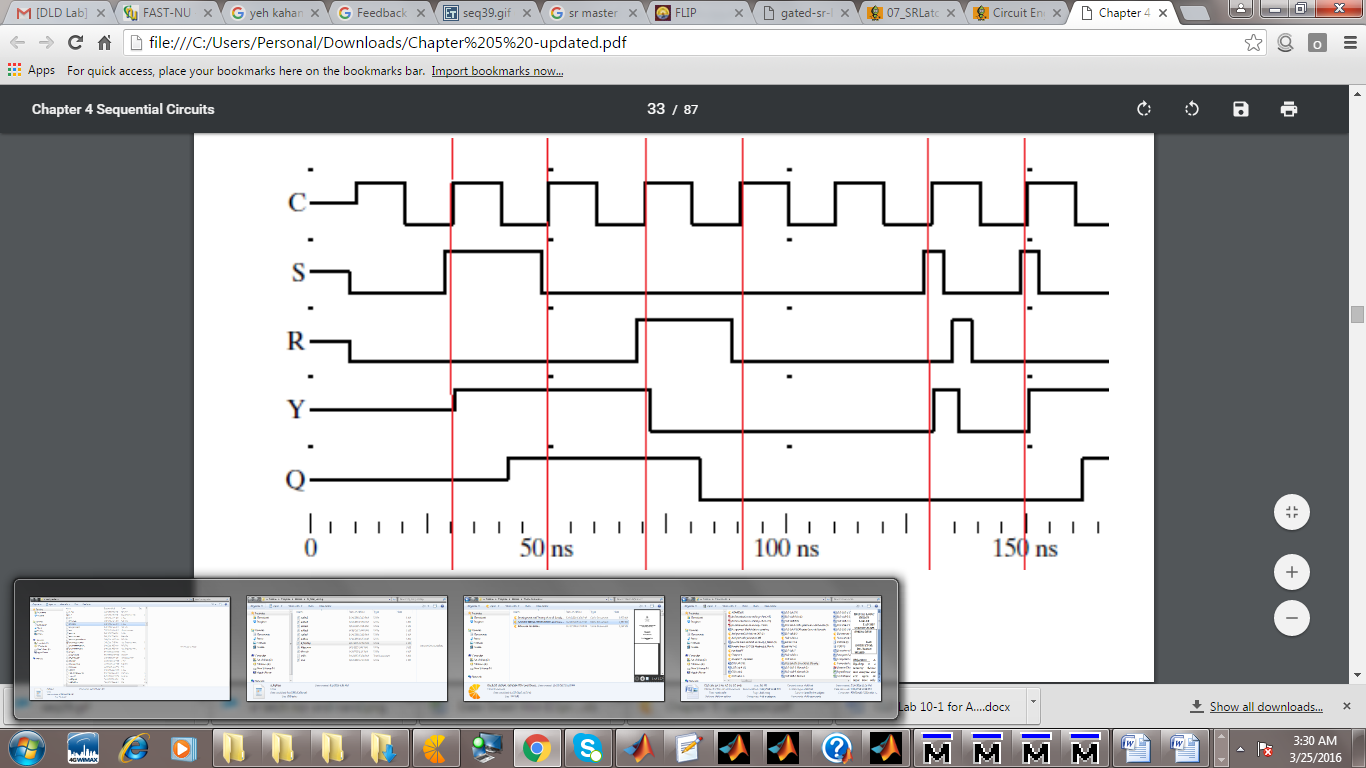
***Note:***

* *Draw the Combinational Circuit diagram using NAND & NOT gates.*
* *For clock pulse (CP) use “clock” component available in Logic works.*
* *Label the diagram properly*

**Logic Diagram:**



**Timing Diagram:**



**Lab Task 2:**

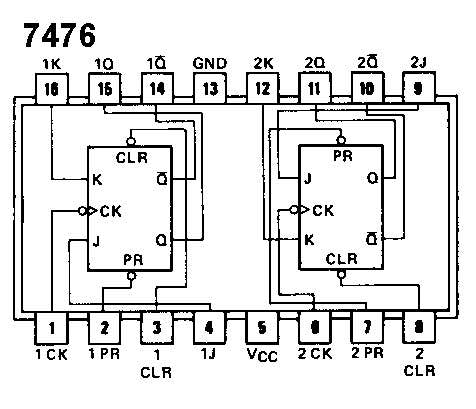
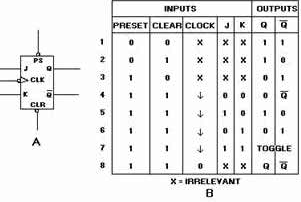
Perform on Logic Works and test the ICs of D-Flip flop & JK flip flop so that it fulfils their tables (get familiar with inputs & outputs).

**Lab Task 3:**

Perform on Logic Works by using IC of JK-Flip flop and construct master-slave flip flop using JK flip flop IC.

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***D FF IC***

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***JK FF IC***